Self-Recovery Experiments in Extreme Environments Using a Field Programmable Transistor Array

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Abstract

Temperature and radiation tolerant electronics, as well as long life survivability are key capabilities required for future NASA missions. Current approaches to electronics for extreme environments focus on component level robustness and hardening. However, current technology can only ensure very limited lifetime in extreme environments. This paper describes novel experiments that allow adaptive in-situ circuit redesign/reconfiguration during operation in extreme temperature and radiation environments. This technology would complement material/device advancements and increase the mission capability to survive harsh environments. The approach is demonstrated on a mixed-signal programmable chip (FPTA-2), which recovers functionality for temperatures until $280^\circ C$ and with total radiation dose up to 250kRad.

1. Introduction

Long-life space missions and extreme environments have characteristics such as high radiation level (Europa Surface and Subsurface mission, 5 MRad), high temperature (Venus Surface Exploration and Sample Return mission, 460°C) and low temperature (Titan in-situ mission, -180°C). Such missions and environments have dictated the need for new electronics technologies.

Material and circuit solutions have been employed for high temperature environments. Materials used up to 300°C include bulk silicon and silicon-on-insulator (SOI) technologies; for higher temperatures, gallium arsenide (GaAs), silicon carbide (SiC), and diamond show promise, and devices have been demonstrated at 500°C. Circuit solutions that compensate offset voltage and current leakage problems are described for example in [1].

Electrons and protons in space can also cause permanent damage in electronic devices that can lead to operational failure. Particularly, Single Event Effects (SEE) are radiation induced errors in microelectronic circuits caused when charged particles lose energy by ionizing the medium through which they pass. One technique for environments with high levels of radiation is the use of Radiation Hard technologies such as Silicon on Insulator (SOI), which allows compensating for the effect of radiation. However, the fabrication cost associated with extreme environment electronics is high.

A number of researchers in the literature have examined the effect of radiation on CMOS devices [2,3]. However, most of these researchers seem to have focused on technologies which are above 0.5 micron and hence the effects could not be generalized to devices implemented in the latest Deep Sub Micron (DSM) technologies, where leakage currents dominate. In addition, no research has been carried out on the development of custom reconfigurable architectures implemented at transistor level hence enabling the implementation of both analogue and digital circuits.

The present approach for extreme environment space electronics designs is to use commercial/military range electronics protected with passive (insulation) or active thermal control, and high weight shielding for radiation reduction. This adds to sizable weight and volume, compounded by power loss and additional cost for

the mission. More importantly, as missions will target operations with smaller instruments/rovers and operations in areas without solar exposure, these approaches become infeasible.

In this paper we will present another technique, based on Evolvable Hardware, for electronic survivability in high temperature and radiation environments. A reconfigurable chip developed at JPL, the Field Programmable Transistor Array (FPTA-2) chip, is used in the experiments described in this paper. We submitted this chip to high temperature and radiation using JPL facilities. We show that the correct functionality of some circuits, such as half-wave rectifiers and low-pass filters, can be recovered using Evolutionary Algorithms. The Evolutionary Algorithms control the state of about 1,500 switches. Using a population of about 500 candidates and after running the Evolutionary process for about 200 generations, the correct functionality is recovered.

The rest of this paper is structured as follows: Section 2 reviews evolutionary design of circuits. Section 3 reviews the Evolvable System. Section 4 describes the testbeds used during high temperature and radiation tests. Section 5 describes the results obtained. Section 6 presents discussions on the results. Finally, the main conclusions of the work are listed in section 7.

2. Evolutionary Circuit Design

The genetic search in EHW is tightly coupled with a coded representation that associates each circuit to a "genetic code" or chromosome. The simplest representation of a chromosome is a binary string, a succession of 0s and 1s that encode a circuit. The status of the switches (ON or OFF) determines a circuit topology and consequently a specific response. Thus, the topology can be considered as a function of switch states, and can be represented by a binary sequence, such as "1011...", where a '1' is associated to a switch turned ON and a '0' to a switch turned OFF.

First, a population of chromosomes is randomly generated. The chromosomes are converted into circuit models for evaluation in SW (extrinsic evolution) or into control bitstrings downloaded to programmable hardware (intrinsic evolution). Circuit responses are compared against specifications, and individuals are ranked based on how close they come to satisfying them. In preparation for a new iteration, a new population of individuals is generated from the pool of best individuals in the previous generation. This is subject to a probabilistic selection of individuals from a best individuals pool, followed by two operations: random swapping of parts of their chromosomes, the *crossover* operation, and random flipping of chromosome bits, the *mutation*

operation. The process is repeated for several generations, resulting in increasingly better individuals. Randomness helps to avoid getting trapped in local optima. Monotonic convergence (in a loose Pareto sense) can be forced by unaltered transference to the next generation of the best individual from the previous generation. There is no theoretical guarantee that the global optimum will be reached in a useful amount of time; however, the evolutionary/genetic search is considered by many to be the best choice for very large, highly unknown search spaces. The search process is usually stopped after a number of generations, or when closeness to the target response has reached a sufficient degree. One or several solutions may be found among the individuals of the last generation.

Currently, the evolutionary search for a circuit solution is performed either using software simulations or directly in hardware on reconfigurable chips. However, software simulations take too long for practical purposes, since the simulation time for one circuit is multiplied by the large number of evaluations required by evolutionary algorithms. In addition the resulting circuit may not be easily implemented in hardware, unless implementation constraints are imposed during evolution. Hardware evaluations can reduce by orders of magnitude the time to get the response of a candidate circuit, potentially reducing the evolution time from days to seconds.

Hardware evaluations commonly use commercial re-configurable devices, such as Field Programmable Gate Arrays (FPGA) or Field Programmable Analog Arrays (FPAA) [4]. These devices, designed for several applications other than EHW, lack evolution-oriented features, and, in particular the analog ones, are sub-optimal for EHW applications. The next section describes the reconfigurable chip developed at JPL, particularly targeted for EHW experiments.

More details on Evolutionary Circuit Design can be found in [4-6].

3. Evolvable System

An evolvable hardware system is constituted of two main components: the Evolutionary Processor (EP) and the Reconfigurable Hardware (RH). The evolutionary processor that runs the evolutionary algorithm can be implemented on a variety of platforms including supercomputer, single PC (most of researchers), DSP (JPL), FPGA and ASIC. The RH can be approached as simulated SPICE models (extrinsic evolution), FPGAs, FPAAs and FPTAs (JPL).

A complete stand-alone board-level evolvable system (SABLES) is built by integrating the FPTA and a DSP implementing the Evolutionary recovery algorithm [7]. The system is connected to the PC only for the purpose of receiving specifications and

10

communicating back the result of evolution for analysis. The system fits in a box 8" x 8" x 3". Communication between DSP and FPTA is very fast with a 32-bit bus operating at 7.5MHz. The FPTA can be attached to a Zif socket attached to a metal electronics board to perform extreme temperature and radiation experiments The evaluation time depends on the tests performed on the circuit. Many of the tests attempted here require less than two milliseconds per individual, and runs of populations of 100 individuals from 100 to 200 generations require only 20 seconds. A block diagram of the evolutionary platform is shown in Figure 1.
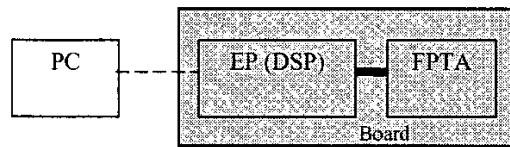

Figure 1: Block diagram of a simple stand-alone evolvable system.

The FPTA is an evolution-oriented reconfigurable architecture (EORA). It has a configurable granularity at the transistor level. It can map analog, digital and mixed signal circuits. The architecture of the FPTA consists of an 8x8 array of re-configurable cells. Each cell has a transistor array as well as a set of programmable resources, including programmable resistors and static capacitors. Figure 2 provides a broad view of the chip architecture together with a detailed view of the reconfigurable transistor array cell. The re-configurable circuitry consists of 14 transistors connected through 44 switches. The re-configurable circuitry is able to implement different building blocks for analog processing, such as two and three stages OpAmps, logarithmic photo detectors, or Gaussian computational circuits. It includes three capacitors, Cm1, Cm2 and Cc, of 100fF, 100fF and 5pF respectively. Control signals come on the 9-bit address bus and 16-bit data bus, and access each individual cell providing the addressing mechanism for downloading the bit-string configuration of each cell. A total of ~5000 bits is used to program the whole chip. The pattern of interconnection between cells is similar to the one used in commercial FPGAs: each cell interconnects with its north, south, east and west neighbors.

The rationale of the Evolvable Hardware approach is to mitigate drifts, degradation, or damage on electronic devices in extreme environments by using re-configurable devices and adaptive self-reconfiguration of the circuit topology. Normally circuits are designed to exploit device characteristics within certain temperature/radiation range; when that is exceeded, the circuit function gradually degrades. In the case of a reconfigurable devices, although the device parameters change in extreme environments, a new circuit design, suitable for new parameters, may be mapped into the reconfigurable device to reproduce the initial circuit function. The new designs, suitable for various environmental conditions, can be determined prior to operation (flight) or determined in-situ by reconfiguration or Evolutionary Algorithms. In-situ device reconfiguration with Evolutionary Algorithms is more effective than previous design determination, because the combined effects of radiation and temperature on the devices is hard to model.

4. Experimental Testbeds

A high temperature testbed was built to achieve temperatures exceeding 350°C on the die of the FPTA-2 while staying below 280°C on the package. It is necessary to stay below 280°C on the package in order not to destroy the interconnects and package integrity. Die temperatures should stay below 400°C to make sure die attach epoxy does not soften and that the crystal structure of the aluminum core does not soften. To achieve these high temperatures, the testbed includes an Air Torch system. The Air Torch is firing hot compressed air through a small hole of a high temperature resistance ceramic protecting the chip. To measure temperature, Thermocouples were used. Figure 3 shows the Air Torch apparatus electronically controlled by PID controller, which maintains a precision of ±10° C up to 1000° C. Figure 3 shows also the ceramic protecting the die connections and the package. The Temperature was measured above the die and under the die using thermocouples.

In the case of the radiation experiments, the radiation source used was an electron beam obtained from a dynamitron accelerator. The electrons are accelerated at an energy of 1 MeV in a small vacuum chamber with a beam of of 8". The fluxes in the small chamber was 4.E9 [e/(s.cm2)] which is around 300 rad/sec. The chips were exposed to radiation doses ranging from 0 to 350Krad at 50Krad steps. Figure 4 illustrates the incremental radiation profile to which the chips were subjected to over a period of 7 days.
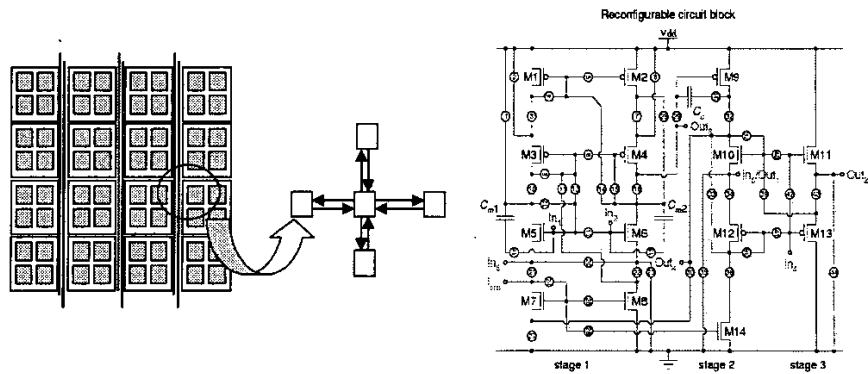
Figure 2: FPTA 2 architecture (left) and schematic of cell transistor array (right). The cell contains additional capacitors and programmable resistors (not shown).
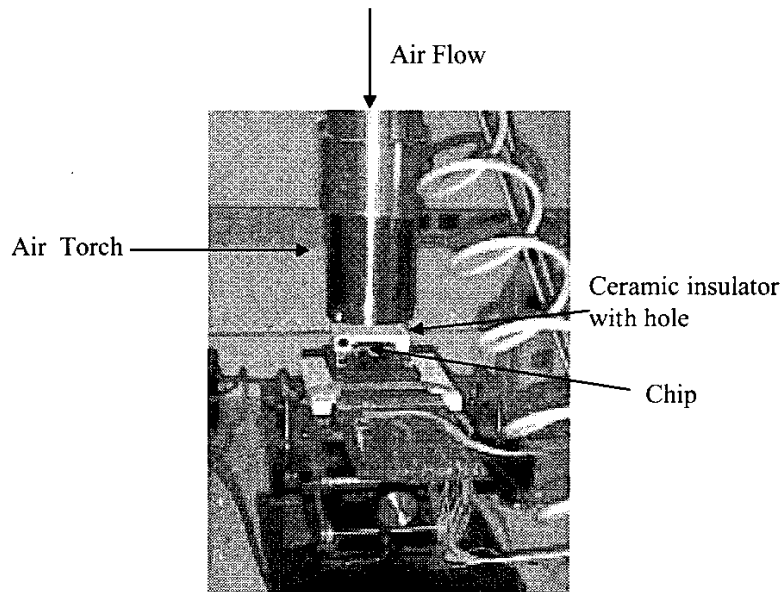

Figure 3: Experimental Setup for Extreme Temperature Experiments using the FPTA-2.
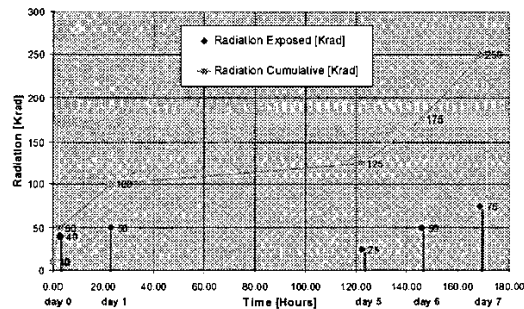

Figure 4: Cumulative radiation and experimental schedule.

12

5. Results

We describe here experiments for evolutionary recovery of the functionality of the following circuits:

- Halfwave Rectifier at 280°C
- Low Pass Filters at 230°C
- Halfwave rectifier at 175 and 250kRads

5.1 Half wave rectifier on FPTA-2 at 280°C

The objective of this experiment is to recover functionality of a half wave rectifier for a 2kHz sine wave of amplitude 2V using only two cells of the FPTA-2 at 280°C. The fitness function given below does a simple sum of error between the target function and the output from the FPTA.

The input was a 2kHz excitation sine wave of 2V amplitude, while the target waveform was the rectified sine wave. The fitness function rewarded those individuals exhibiting behavior closer to target (by using a sum of differences between the response of a circuit and the target) and penalized those farther from it. The fitness function was:

$$F = \sum_{t_s=0}^{n-1} \begin{cases} R(t_s) - S(t_s) & \text{for } (t_s < n/2) \\ R(t_s) - V_{max}/2 & \text{otherwise} \end{cases} \quad (1)$$

where $R(t_s)$ is the circuit output, $S(t_s)$ is the circuit stimulus, n is the number of sampled outputs, and V_{max} is 2V (the supply voltage). The output must follow the input during half-cycle, staying constant at a level of half way between the rails (1V) in the other half.

After the evaluation of 100 individuals, they were sorted according to fitness and a 9% (elite percentage) portion was set aside, while the remaining individuals underwent crossover (70% rate), either among themselves or with an individual from the elite, and then mutation (4% rate). The entire population was then reevaluated. Only two cells of the FPTA were allocated and used in this experiment.

Figure 5 depicts the response of the evolved circuit at room temperature and the degraded response at high temperature. Figure 6 shows the response of circuit obtained by running evolution at 280°C, where we can see that the functionality is recovered.
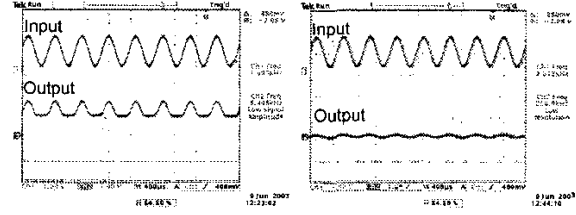

Figure 5: Input and output waves of the half-wave rectifier. At the left we show the response of the circuit evolved at 27°C. At the right we show the degraded response of the same circuit when the temperature is increased to 280°C.
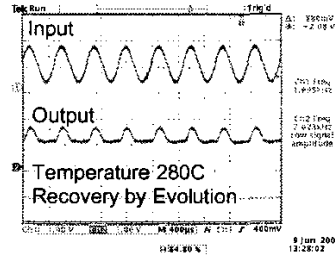

Figure 6 The solution for the Halfwave rectifier at 280°C.

5.2 Low-Pass Filter on FPTA-2 at 230°C

The objective of this experiment is to recover the functionality of a low-pass filter given ten cells of the FPTA-2. The fitness function given below performs a sum of error between the target function and the output from the FPTA in the frequency domain.

$$F = \sum_{f_s=0}^{n-1} (R(f) - T(f)) \quad (2)$$

Given two tones at 1kHz and 10kHz, the objective is to have at the output only the lowest frequency tone (1kHz). This hardware evolved circuit demonstrated that the FPTA-2 is able to recover active filters with some gain at 230°C.

Figure 7 shows the response of the evolved filter at room temperature and degradation at 230°C. Figure 8 shows the time response of the recovered circuit evolved at 230°C.
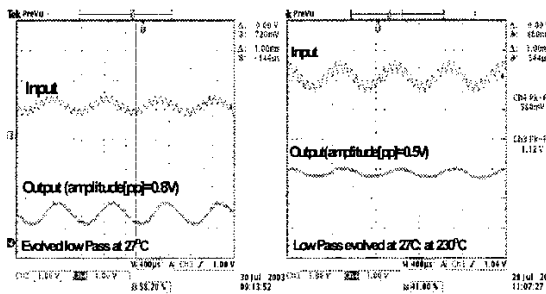
13

Figure 7: Low-Pass Filter. The graph in the left displays the input and output signals in the time domain. The graph in the right shows the input and output in the time domain when the FPTA-2 was submitted to temperature of 230°C. (Circuit stimulated by two sine waves: 1kHz and 10kHz).
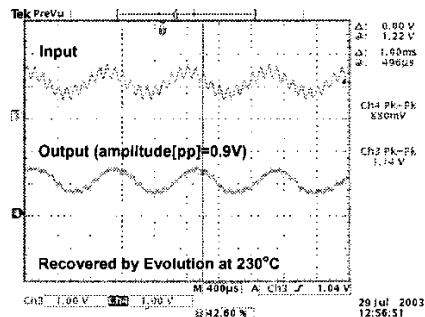

Figure 8: Recovered Low Pass Filter

At room temperature, the originally evolved circuit presents a gain of 3dB at 1kHz and a roll-off of -14dB/dec. When the temperature is increased to 230°C, the roll-off goes to -4dB/dec and the gain at 1kHz falls to -12dB. In the recovered circuit at high temperature the gain at 1kHz is increased back to 1dB and the roll-off goes to -7dB/dec. Therefore the evolved solution at high temperature is able to restore the gain and to partially restore the roll-off.

In the case of temperature experiments, it was verified that the circuit evolved for high temperatures usually does not work when the temperature is lowered down.

5.3 Half Wave Rectifier at 175krads and 250krads

This section describes the recovery of a half wave rectifier after the FPTA-2 is submitted to radiation.

Figure9(a) illustrates the response of a previously evolved rectifier after the chip is exposed to a radiation dose of 50krad. It can be observed that the circuit response is not affected by radiation. After exposure to radiation of up to 175Krad the rectifier malfunctions as the output response is identical to that of the input shown on Figure 9(b). When the evolutionary mechanism is activated, the correct output response is retained as shown in Figure 9(c).

Figure 10 illustrates the recovery process when the dosage is increased to 250Krad. It can be seen that the output response is clearly distorted due to radiation. However, the correct output response is recovered once the evolutionary mechanism takes over, even though the final circuit suffers from some non-ideal behavior when the output is low.

6. Discussion

In the current experiments, the evolutionary algorithms was run on another chip (DSP), which was not subject to extreme environment conditions. In the near future it is planned to integrate the FPTA and the DSP together. In this case the expectation is that the digital circuitry will degrade later then analog, which is more sensitive than digital. In addition, the digital circuitry may use a large variety of standard fault tolerance techniques.

As previously remarked, the achieved circuit solutions work only at the particular temperature in which they were evolved, i.e., they are not robust to large temperature variations. In a previous work [8], a robust circuit was evolved in an FPGA , operating correctly in a limited temperature range (from -27°C to 60°C). Nevertheless, this approach to evolve robust circuits in hardware would not be effective in the case of in-situ evolution during flight, because it would require two chips, one at normal temperature and another at extreme temperature, undergoing evolution simultaneously. Likewise, off-line evolution in software (using SPICE models) would not be effective as well, due to the lack of accurate MOS transistor models for very high temperatures .
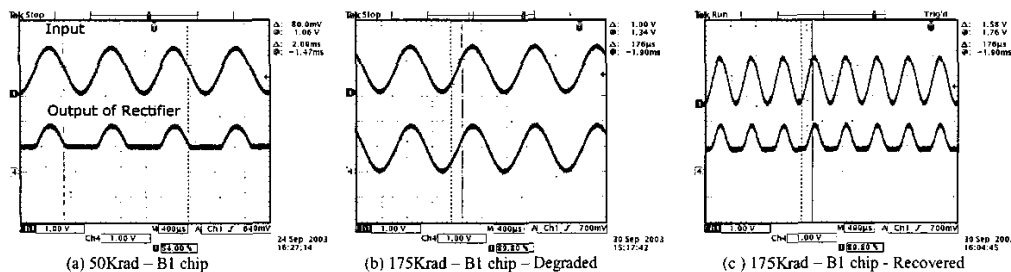
14

(a) 50Krad – B1 chip   (b) 175Krad – B1 chip – Degraded   (c) 175Krad – B1 chip - Recovered

Figure 9: Response of the Rectifier circuit at (a) 50kRads, (b) after being radiated to 175kRads resulting in deterioration through loss of rectification, followed by (c) recovery through Evolution.
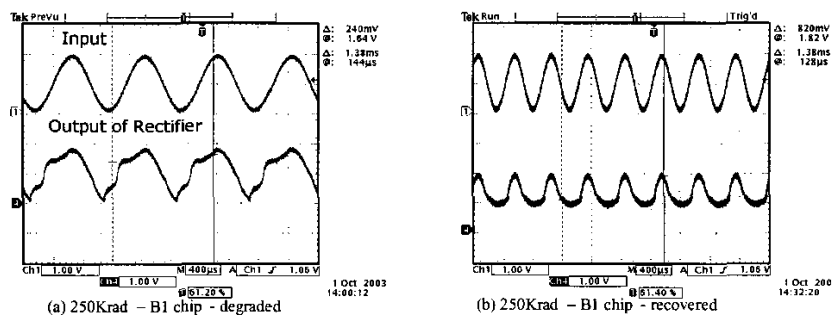

(a) 250Krad – B1 chip - degraded   (b) 250Krad – B1 chip - recovered

Figure 10: Response of the Rectifier circuit at (a) 250kRads resulting in distortion, followed by (b) recovery through Evolution

7. Conclusions

The paper has presented a mechanism for adapting a mixed analogue reconfigurable platform for high temperature and radiation induced faults. Different experiments were carried out which exercised the reconfigurable device up to 280°C and 250Krad radiation dosages demonstrating that the technique is able to recover functionality of blocks such as rectifiers and filters.

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15

16